CS315_02 Advanced Architecture

Project07

Advanced Arch

Digital Design

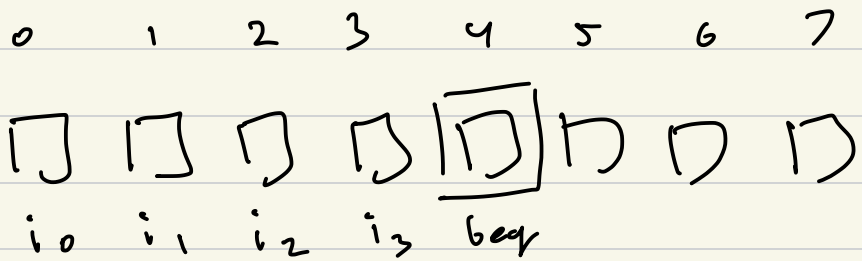
Schematic Design

HDL Hardware Description Languages

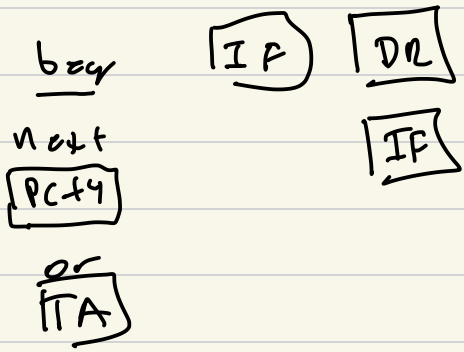
Verilog VHDL (IEEE)

PyHDL CHISEL (Scala)

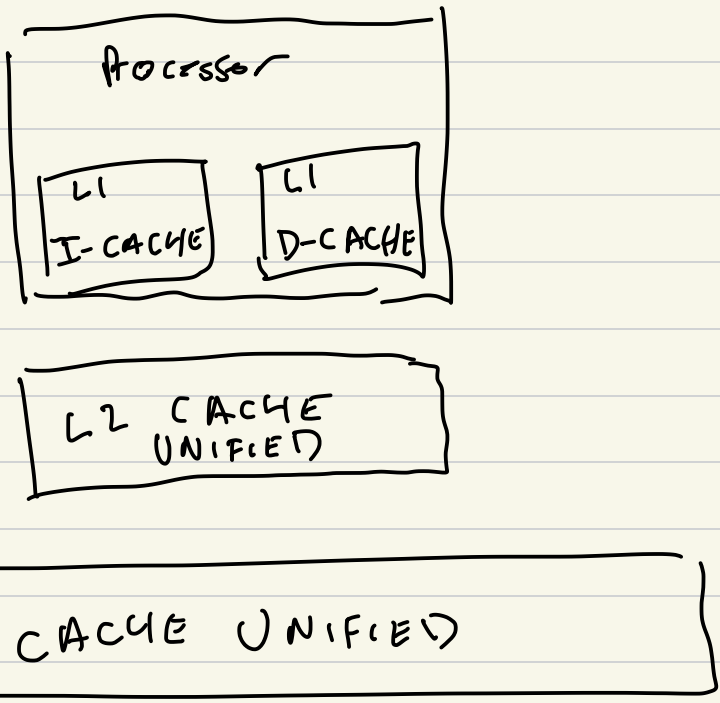
Pipelining



Branch Prediction



Caches



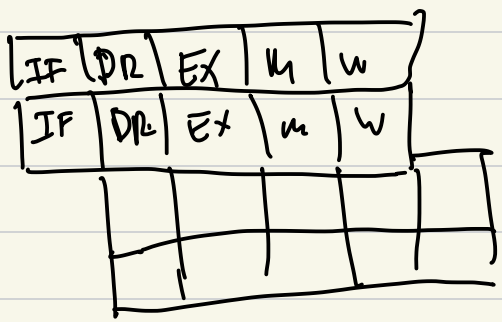
Super Scalar Execution

Multiple issue

Two pipeline

add t0, t1, t2

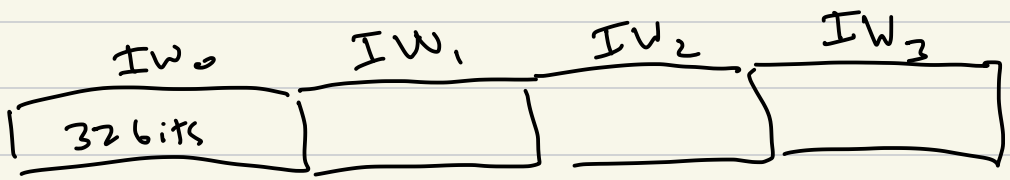
sub a0, a1, a2



VLIW - Very Large Instruction Word

EPIC - Explicitly Parallel Instruction Comp (Intel)

Itanium



Out of Order execution

```
ld  t0, (t1)
add t2, t3, t4
mul s0, s1, s2
```

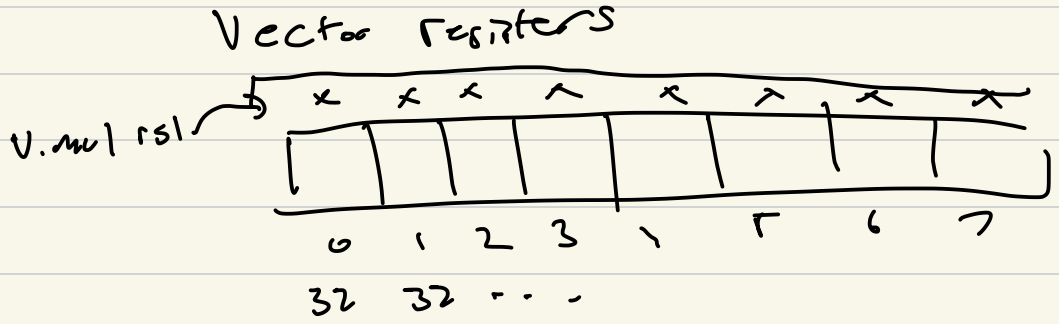
Commit stage

Speculative Execution

Multicore

Vector Instructions SIMD

single instruction multiple data



GPUs